CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Cancelled)

35. (Cancelled)

36 (New). A method comprising:

determining at a computer device a first direction associated with a circuit layout;

selecting at the computer device a first portion of a first transistor of the circuit layout in response to determining the first portion extends outward in the first direction from a first logical device of the circuit layout, the first logical device comprising the first transistor;

in response to selecting the first portion, reshaping at the computer device the first transistor to reduce a size of the first logical device in the first direction;

reshaping at the computer device a second portion of the first logical device in response to reducing the size of the first logical device.

37. (New) The method of claim 36, wherein the first portion of the first transistor comprises a first transistor finger.

38. (New) The method of claim 37, wherein the second portion of the first logical device comprises a second transistor finger of the first transistor.

39. (New) The method of claim 37, wherein the second portion of the first logical device comprises a transistor finger of a second transistor.

40. (New) The method of claim 37, wherein reshaping the first portion comprises reducing a size of the first transistor finger.

41. (New) The method of claim 37, wherein reshaping the first portion comprises removing the first transistor finger.

42. (New) The method of claim 36, wherein reshaping the first portion comprises rotating the first transistor.

43. (New) The method of claim 36, further comprising reshaping a third portion of the first logical device in response to reducing the size of the first transistor portion.

44. (New) The method of claim 36, further comprising:

storing a first state associated with the circuit layout at the computer device in response to selecting the first portion of the first transistor;

in response to reshaping the first portion of the first transistor, determining if a size of the circuit layout has been reduced; and

in response to determining the size of the circuit layout has not been reduced, restoring the circuit layout to the first state.

45. (New) The method of claim 44, wherein determining if the size of the circuit layout has been reduced comprises determining if the size of the circuit layout has been reduced in the first direction.

46. (New) The method of claim 36, further comprising

selecting at the computer device a third portion of a second transistor of the circuit layout in response to determining the third portion extends outward in the first direction from a second logical device of the circuit layout, the second logical device comprising the second transistor;

in response to selecting the third portion, reshaping at the computer device the third portion of the second transistor to reduce a size of the second logical device in the first direction;

reshaping at the computer device a fourth portion of the second logical device in response to reducing the size of the second logical device.

47. (New) The method of claim 36, further comprising

determining at the computer device a second direction associated with the circuit layout;

selecting at the computer device a third portion of a second transistor of the circuit layout in response to determining the third portion extends outward in the second direction from a second logical device of the circuit layout, the second logical device comprising the second transistor;

in response to selecting the third portion, reshaping at the computer device the third portion of the second transistor to reduce a size of the second logical device in the second direction;

reshaping at the computer device a fourth portion of the second logical device in response to reducing the size of the second logical device.

48. (New). A method comprising:

determining at a computer device a first direction associated with a circuit layout;

selecting at the computer device a first portion of a first transistor of the circuit layout in response to determining the first portion is at an edge of a first logical device of the circuit layout, the first logical device comprising the first transistor;

in response to selecting the first portion, reshaping at the computer device the first transistor to reduce a size of the first logical device in the first direction;

reshaping at the computer device a second portion of the first logical device in response to reducing the size of the first logical device.

49. (New) The method of claim 48, wherein the first portion of the first transistor comprises a first transistor finger and the first logical device comprises a chain of transistors.

50. (New) The method of claim 49, wherein the second portion of the first logical device comprises a second transistor finger of the first transistor.

51. (New) The method of claim 49, wherein the second portion of the first logical device comprises a transistor finger of a second transistor.

52. (New) The method of claim 49, wherein reshaping the first portion comprises reducing a size of the first transistor finger.

53. (New) The method of claim 49, wherein reshaping the first portion comprises removing the first transistor finger.

54. (New) The method of claim 49, wherein reshaping the first portion comprises rotating the first transistor.

55. (New) The method of claim 48, further comprising reshaping a third portion of the first logical device in response to reducing the size of the first transistor portion.

56. (New) The method of claim 48, further comprising:

storing a first state associated with the circuit layout at the computer device in response to selecting the first portion of the first transistor;

in response to reshaping the first portion of the first transistor, determining if a size of the circuit layout has been reduced; and

in response to determining the size of the circuit layout has not been reduced, restoring the circuit layout to the first state.

57. (New) The method of claim 56, wherein determining if the size of the circuit layout has been reduced comprises determining if the size of the circuit layout has been reduced in the first direction.

58. (New) The method of claim 48, further comprising

selecting at the computer device a third portion of a second transistor of the circuit layout in response to determining the third portion is at an edge of a second logical device of the circuit layout, the second logical device comprising the second transistor;

in response to selecting the third portion, reshaping at the computer device the third portion of the second transistor to reduce a size of the second logical device in the first direction;

reshaping at the computer device a fourth portion of the second logical device in response to reducing the size of the second logical device.

59. (New) The method of claim 48, further comprising

determining at the computer device a second direction associated with the circuit layout;

selecting at the computer device a third portion of a second transistor of the circuit layout in response to determining the third portion is at an edge of a second logical device of the circuit layout, the second logical device comprising the second transistor;

in response to selecting the third portion, reshaping at the computer device the third portion of the second transistor to reduce a size of the second logical device in the second direction;

reshaping at the computer device a fourth portion of the second logical device in response to reducing the size of the second logical device.

60. (New). A method comprising:

determining at a computer device a first direction associated with a circuit layout;

selecting at the computer device a first portion of a first transistor of the circuit layout in response to determining the first portion is not at an edge of a first logical device of the circuit layout, the first logical device comprising the first transistor;

in response to selecting the first portion, reshaping at the computer device the first transistor to reduce a size of the first logical device in the first direction;

reshaping at the computer device a second portion of the first logical device in response to reducing the size of the first logical device.

61. (New) The method of claim 60, further comprising:

selecting a third portion of the first transistor in response to determining the third portion is adjacent to the first portion; and

in response to selecting the third portion, reshaping at the computer device the first transistor to reduce a size of the first logical device in the first direction.

62. (New) The method of claim 61, wherein the first portion of the first transistor comprises a first transistor finger and the first logical device comprises a chain of transistors.

63. (New) The method of claim 62, wherein the second portion of the first logical device comprises a second transistor finger of the first transistor.

64. (New) The method of claim 62, wherein the second portion of the first logical device comprises a transistor finger of a second transistor.

65. (New) The method of claim 62, wherein reshaping the first portion comprises reducing a size of the first transistor finger.

66. (New) The method of claim 62, wherein reshaping the first portion comprises removing the first transistor finger.

67. (New) The method of claim 62, wherein reshaping the first portion comprises rotating the first transistor.

68. (New) The method of claim 62, further comprising reshaping a third portion of the first logical device in response to reducing the size of the first transistor portion.

69. (New) The method of claim 62, further comprising:

storing a first state associated with the circuit layout at the computer device in response to selecting the first portion of the first transistor;

in response to reshaping the first portion of the first transistor, determining if a size of the circuit layout has been reduced; and

in response to determining the size of the circuit layout has not been reduced, restoring the circuit layout to the first state.

70. (New) The method of claim 69, wherein determining if the size of the circuit layout has been reduced comprises determining if the size of the circuit layout has been reduced in the first direction.